Amendment to the Specification

Please replace the paragraph beginning on page 1, line 5 with the amended paragraph below.

This invention relates to semiconductor integrated devices and, more particularly, to semiconductor memory devices providing increased memory speed, performance and robustness within a highly compact memory cell layout.[[.]]

Please replace the paragraph beginning on page 26, line 15 with the amended paragraph below.

Various types of subsystems may be integrated within system ~~70~~ 700 including microprocessor and micro-controller cores, digital signal processors (DSPs), communication cores, sound and video cores, radio frequency (RF) cells, power management, and high-speed interfaces, among others. A plurality of transmission lines (not shown) may then be used for interconnecting the subsystems and/or for connecting particular subsystems to one or more memory blocks. In the current embodiment, the plurality of transmission lines (otherwise referred to as chip-level signal and power lines) are routed between the VSS_2 lines within the chip-level routing layer. Various types of transmission lines may be integrated within system ~~70~~ 700 including input/output (I/O) lines, clocking lines, intra-system signal lines, and power and ground supply lines.

Please replace the paragraph beginning on page 30, line 1 with the amended paragraph below.

FIG. 11A provides a magnified view of the active regions, isolation regions, gate structures and contact structures, which may be used to form the NMOS and PMOS transistors of a dual-port memory cell. As shown in FIG. 11A, the dual-port memory cell (located, e.g., within row R_{X+1}, column C_X of layout 1100) includes two NMOS active regions and two PMOS active regions. Each of the NMOS active regions comprises a latch transistor and two access transistors. For example, polysilicon segments 1110A, 1110B and 1110C are arranged above N-type diffusion region 1120 to form the gate structures of access transistors T3, T5 and latch transistor $T1_N$. Polysilicon segments 1110A, 1110B′ and 1110C′ are arranged above N-type diffusion region 1130 to form the gate structures of access transistors T4, T6 and latch transistor $T2_N$. In addition, each of the PMOS active regions comprises a latch transistor. For example, polysilicon segments 1110C and 1110C′ also extend across P-type diffusion regions 1140 and 1150 to form the gate structures of latch transistors $T1_P$ and $T2_P$, respectively.